

NU-01007

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REMARKS

Claims 1 - 4 and 6 - 10 are currently pending in the application. By this amendment, claims 11 - 15 are added for the Examiner's consideration. The foregoing separate sheets marked as "Listing of Claims" shows all the claims in the application, with an indication of the current status of each.

In the specification, the paragraph beginning at page 6, line 15 has been amended to correct a typographical error. The buffer is a 'reorder buffer' and not a 'registration order buffer' as previously indicated. The paragraph beginning on page 14, line 23 describes how the buffer is used to rearrange or **reorder** the sequence of instructions. Hence the correct name of ROB is Reorder Buffer and not registration order buffer.

In the specification, the paragraph beginning at page 14, line 23 has been amended to correct a typographical error.

Claims 11 - 15 have been added to correspond to the allowed claims of the related basic priority Japanese patent application No. 2000-153452.

These new claims are fully supported in the specification and do not constitute new matter. Specifically, the 'reorder buffer' of claim 11 corresponds to ROB 21. Also, 'first buffer' and 'second buffer' correspond to operation buffer 22 and memory access instruction buffer 23, respectively. Further, 'first instructions' correspond to operation instruction while 'second instructions' correspond to memory access instructions. The first and second buffers both store, among a plurality of instructions, an instruction that should be issued only after the other instructions have been issued. Stated another way, the first and second instructions cannot be distinguished from each other on the basis of whether or not their order is guaranteed. That is why the above new claim 11 does not include a limitation relating to order that distinguishes the first and second orders.

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In accordance with the present invention, the instructions are classified into operation instructions and memory access instructions, as described in the specification on page 5, lines 9 - 16. This clearly indicates that the instructions consist of only operation instructions and memory access instructions. It therefore follows that, ‘second instructions’ are “among the plurality of instructions, instructions other than the first instructions”, as recited in claims 11, 14 and 15.

The feature in claim 11 recited as, “...said second instructions including instructions that should be issued after said first instructions;” is described in the specification on page 20, lines 3 - 11. While the next feature of claim 11 recited as, “...said first buffer including a plurality of first entries for sequentially storing the first instructions in said order of instruction;” is described on page 9, lines 4 - 17.

In addition, the first two steps of the buffer queue control of claim 11 as described in the specification on page 10, lines 2 - 14 and page 11, line 21 through page 14 , line 3 and are shown in FIG. 5 - 7. The third step of this feature is described in the specification on page 11, lines 13 - 20. The configuration of claim 13 is described in the specification on page 11, lines 13 - 20.

In view of the foregoing, it is requested that the application be reconsidered, that claims 1 - 4, and 6 - 15 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at 703-787-9400 (fax: 703-787-7557; email: marshall@wcc-ip.com) to discuss any other changes deemed necessary in a telephonic or personal interview.

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If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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